Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application:

1. (currently amended) An apparatus for processing a received signal containing a datastream, comprising:

a signal decoder ~~(44)~~, the signal decoder ~~(44)~~ generating a first error signal ~~(17)~~ in response to indecipherable data received by the decoder ~~(44)~~; and

a transport processor ~~(60)~~, the transport processor ~~(60)~~ receiving the first error signal ~~(17)~~, the transport processor ~~(60)~~ generating a second error signal ~~(31)~~ after receiving the first error signal ~~(17)~~.

2. (original) The apparatus of claim 1, wherein the datastream comprises a modulated signal containing data packets.

3. (currently amended) The apparatus of claim 2, further comprising:

a transport bus ~~(48)~~, the transport bus ~~(48)~~ forwarding data packets to subsequent processing stages ~~(15)~~; and

at least one synchronization signal ~~(32)~~, the transport processor ~~(60)~~ generating the second error signal ~~(31)~~ in response to receiving the synchronization signal ~~(32)~~.

4. (currently amended) The apparatus of claim 4, wherein the second error signal ~~(31)~~ is forwarded to the transport bus ~~(48)~~ so as to have a synchronized relationship to the data packets being forwarded via the transport bus ~~(48)~~.

5. (currently amended) The apparatus of claim 5, wherein the second error signal ~~(31)~~ is formed as a series of logical high frames, each logical high frame being associated with a data packet.

6. (currently amended) The apparatus of claim 6, wherein the duration of each logical high frame of the second error signal ~~(31)~~ has a duration greater than the data packet associated with the logical high frame.

7. (currently amended) The apparatus of claim 7, wherein each logical high frame of the second error signal ~~(31)~~ begins at an earlier time than the data packet associated with the logical high frame.

8. (currently amended) The apparatus of claim 8, wherein each logical high frame of the second error signal ~~(31)~~ ends at a later time than the data packet associated with the logical high frame.

9. (currently amended) The apparatus of claim 9, further comprising a demodulator ~~(22)~~, the demodulator ~~(22)~~ deriving the synchronization signal ~~(32)~~ from the received signal.

10. (currently amended) The apparatus of claim 1 wherein the transport processor ~~(60)~~ is implemented as a microprocessor ~~(60)~~.

11. (currently amended) A system for generating an error signal based on an error encountered while processing a received signal which includes an image representative datastream containing data packets, comprising:

a forward error detecting and correcting decoder ~~(44)~~ which generates a first error signal ~~(17)~~;

a synchronization signal ~~(32)~~ derived from the received signal;

a transport processor ~~(60)~~ interconnected to receive the first error signal ~~(17)~~ and the synchronization signal ~~(32)~~, the transport processor ~~(60)~~ generating a second error signal ~~(31)~~ in response to the first error signal ~~(17)~~ and the synchronization signal ~~(32)~~.

12. (currently amended) The system of claim 11, further comprising a transport bus ~~(48)~~, the data packets being forwarded to subsequent processing stages ~~(15)~~ via the transport bus ~~(48)~~.

13. (currently amended) The system of claim 12, wherein the second error signal ~~(31)~~ is forwarded via the transport bus ~~(48)~~ simultaneously with the data packets associated with the second error signal ~~(31)~~.

14. (currently amended) The system of claim 13, wherein the data packets are forwarded as a series of discrete spaced apart frames, the second error signal ~~(31)~~ being adapted to indicate an error in a defective data packet by having a duration that spans the frame of the defective data packet.

15. (currently amended) The system of claim 14, wherein the second error signal ~~(31)~~ assumes a logical low state when no error is present in a data packet.

16. (currently amended) The system of claim 15, wherein the forward error detecting and correcting decoder ~~(44)~~ is a Reed-Solomon decoder.

17. (currently amended) The system of claim 11 wherein the transport processor ~~(60)~~ is implemented as a microprocessor ~~(60)~~.

18. (currently amended) In a system for processing a received signal containing an image representative datastream containing data packets, a packet error signal generating method comprising the steps of:

demodulating the received signal to produce a demodulated signal;

error detecting the demodulated signal to produce a first error signal ~~(17)~~;

forwarding the first error signal ~~(17)~~ to a transport processor ~~(60)~~;

forwarding a synchronization signal ~~(32)~~ to the transport processor ~~(60)~~, thereby associating the first error signal ~~(17)~~ with a particular data packet; and

generating a second error signal ~~(31)~~ in response to the synchronization signal ~~(32)~~ being received by the transport processor ~~(60)~~.

19. (currently amended) A method according to claim 17, further comprising the step of generating the second error signal ~~(31)~~ as a series of discrete frames, each frame having a duration greater than an associated data packet.

20. (original) A method according to claim 18, further comprising the steps of:

starting each discrete second error signal frame before an associated data packet begins; and

stopping each discrete second error signal frame after an associated data packet ends.

21. (original) A method according to claim 19, wherein the error detecting step comprises Reed-Solomon error detection and correction.